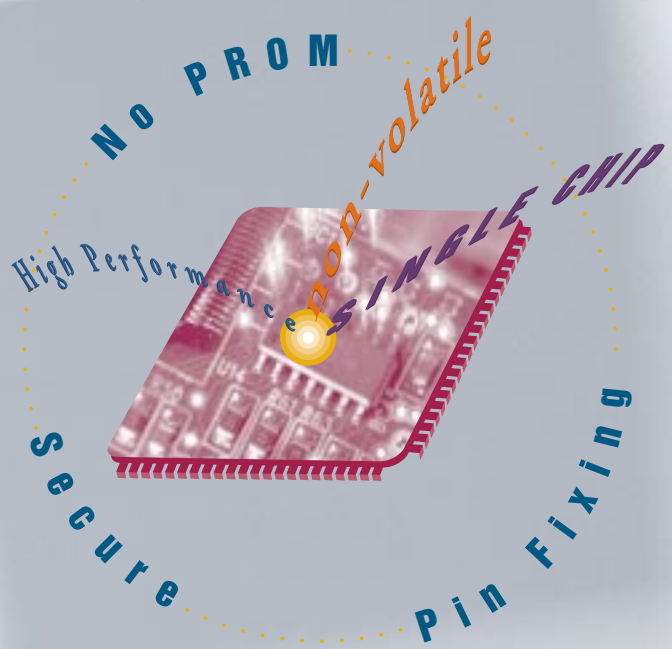
Actel's Antifuse FPGAs

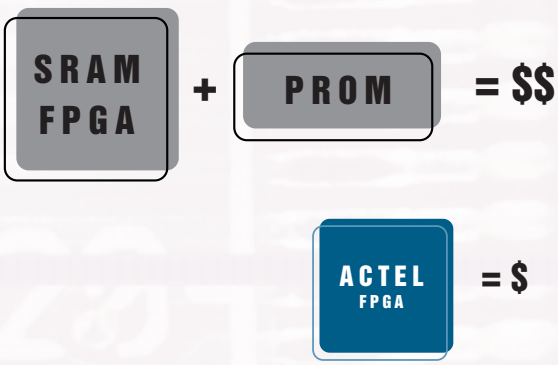
Single Chip High Performance Solutions



Actel

The Antifuse Advantage

Actel's antifuse devices are low cost, high performance solutions for today's logic designer. Ideal for integrating logic typically implemented in multiple CPLDs, PALs, and FPGAs, antifuse devices offer significant cost savings while maintaining high performance. In addition, the Actel antifuse technology ensures design security and gets your design to market faster. Actel antifuse FPGAs, combining low costs and high performance, are the single-chip ASIC alternative.

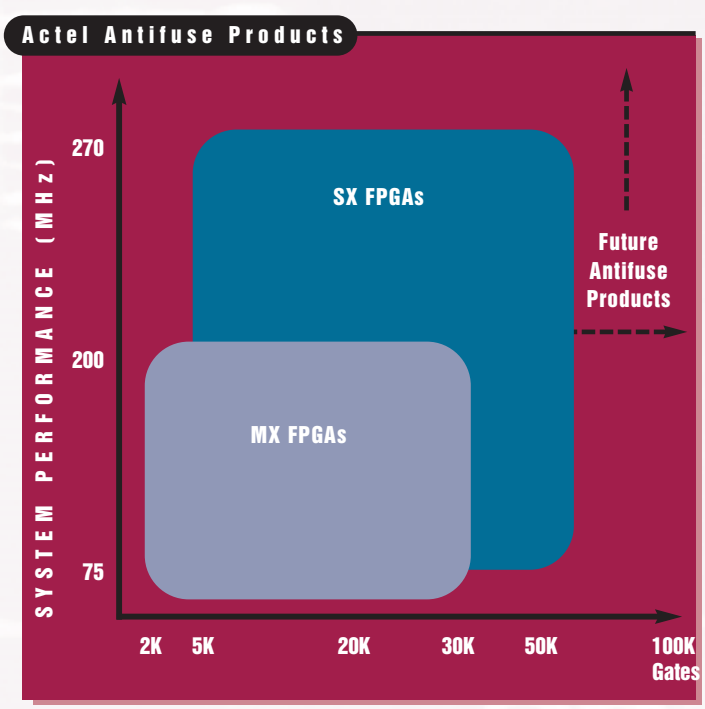


Save Some Money

With a smaller switching element and a smaller die size, Actel's antifuse FPGAs provide a substantial cost advantage over equivalent SRAM FPGAs. Plus, Actel's antifuse FPGAs are nonvolatile, which allows the device to retain its configuration indefinitely and without an external storage device. With no external storage device necessary to hold the devices' configuration data, the cost of a PROM or microprocessor and the associated board space are eliminated, providing additional savings.

Maintain High Performance

Low cost does not mean low performance. With its low resistance and low capacitance properties, Actel's antifuse technology offers very high speeds. And since Actel devices are permanently programmed, they are instantly operational on power-up. There is no boot up period while data is being downloaded from an external device.



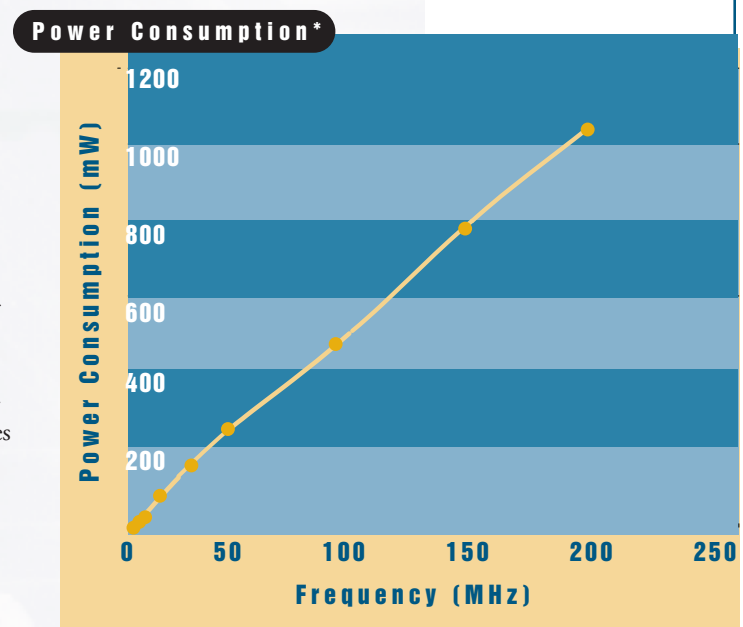
Protect Your Intellectual Property

Design security is a necessity in today's highly competitive technology industry to protect designs from pirating. Actel's antifuse FPGAs offer that security. Actel devices do not need a start up bitstream, eliminating the possibility of configuration data being intercepted. This also prevents in-system errors and accidental data erasures that otherwise may occur during download.

Add to that the inherent security of antifuse technology itself. The antifuses that form the interconnections within an Actel FPGA are extremely small, are densely distributed throughout the device (over 6.5 million on the largest Actel device), and do not leave an observable signature that can be electrically probed or visually inspected. With these safeguards, Actel devices are virtually immune to copying and reverse engineering.

Speed Time to Market

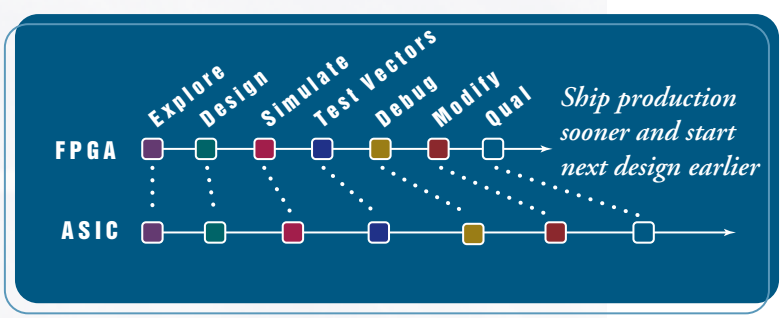
Actel devices offer a host of other benefits that simplify the design cycle and speed the design to market. Using Actel's automatic place and route tools, 100% logic utilization is possible, speeding design time. And Actel's unique general and local routing structure allows 100% pin-locking, even at full logic utilization, so the PCB can be developed concurrently with the FPGA. Even during verification, Actel devices can be analyzed in-system and in real time using the Silicon Explorer diagnostic tool, decreasing verification times.



*Based on a 528 bit Shift Register implemented in an A54SX16P device using 77% of the device.

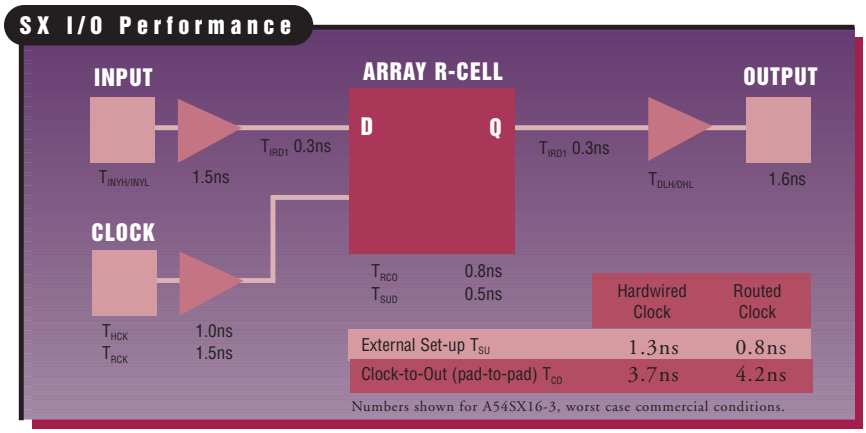
Consume Less Power

An additional benefit of Actel's antifuse technology is its inherent low power consumption. Antifuses have low resistance properties, and the architecture does not require active circuitry to hold a charge, reducing thermal and power supply design problems.



SX FPGAs

Industry's Price/Performance Leader

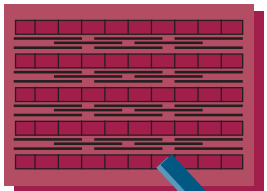


With capacities ranging from 8,000 to 72,000 gates, 270MHz system performance, and prices starting below $5.00, Actel's SX FPGAs are the high performance, low price leader. Featuring a sea-of-modules architecture, SX devices are able to deliver integration at performance levels previously limited to ASICs.

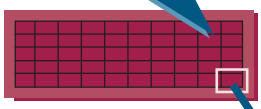
Sea of Modules—An Evolution in Architecture

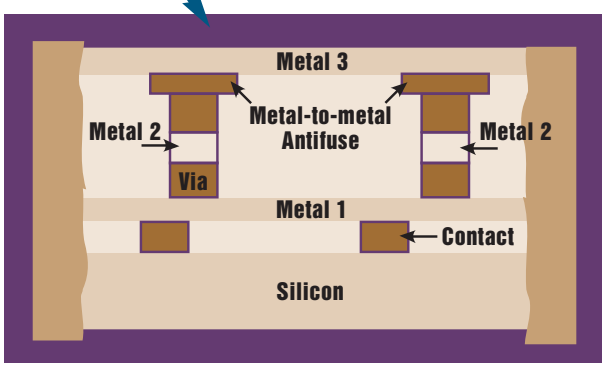
SX's sea-of-modules architecture is enabled by Actel's patented metal-to-metal antifuse interconnect elements. The unique architecture consists of a grid of fine grained logic modules covering the entire floor of the device, reducing the distance signals have to travel between logic modules, and saving almost 1/2 the die size of an equivalent FPGA with a Channel Array architecture. The result is that SX devices cost less overall than FPGAs of comparable density.

Channel Array Architecture



Sea of Modules Architecture





Metal-to-Metal Antifuse

Speed Things Up

To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation, optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. This unique local and general routing structure gives fast and predictable performance, allowing designers to meet their goals with a minimum of effort.

Further complementing the flexible routing structure is a hardwired, constantly-loaded clock network that has been tuned to provide fast clock propagation with a maximum clock skew of only .25ns. With internal clock speeds of 320MHz and clock-to-out of 3.7ns, designs previously limited to ASICs can now be implemented in SX FPGAs.

Performance

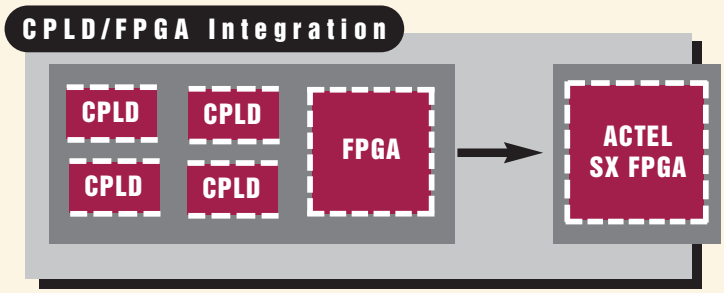
SX devices allow designers to achieve a higher level of performance without using complicated and time consuming performance-enhancing design techniques. With other FPGAs, designers frequently have to use techniques such as redundant logic to reduce fanout on critical nets, introducing data pipelining to reduce register-to-register delays, or the instantiation of custom macros in VHDL or Verilog-HDL code.

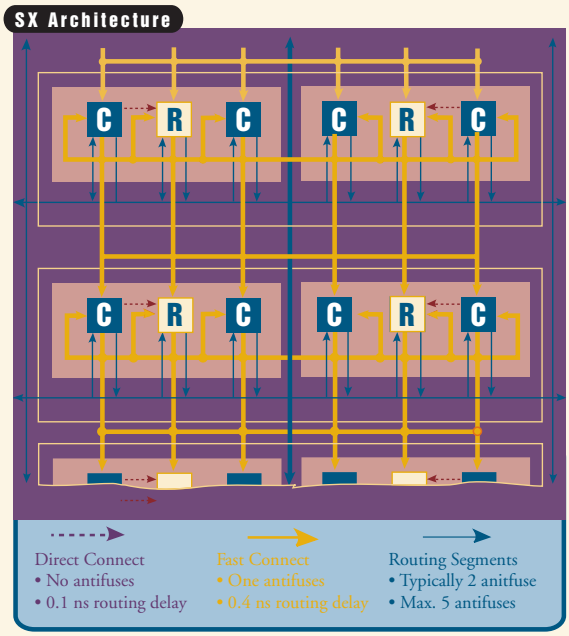
66 MHz PCI Compliance

With the SX family, designers can implement high speed 66MHz PCI applications. In conjunction with SX, Actel offers a suite of intellectual property (IP) cores, intended to enhance time-to-market for programmable logic users.

Integrate Your Gates

Designs that were previously segmented between CPLDs (for speed) and FPGAs (for capacity) can now be easily integrated into a single SX FPGA, improving system reliability and reducing power consumption. And, of course, fewer components means reduced production costs associated with component counts and board space.





SX Applications

- *8b/10b encoder for 1Gigabit Ethernet Router with 125Mbyte/sec sustained data throughput.*
- *66MHz compliant PCI Bus Arbiter with a 6ns clock-to-out and 3ns input set-up time.*
- *52MHz DS3 to DS2 bi-directional converter with 19ns reg-reg timing.*

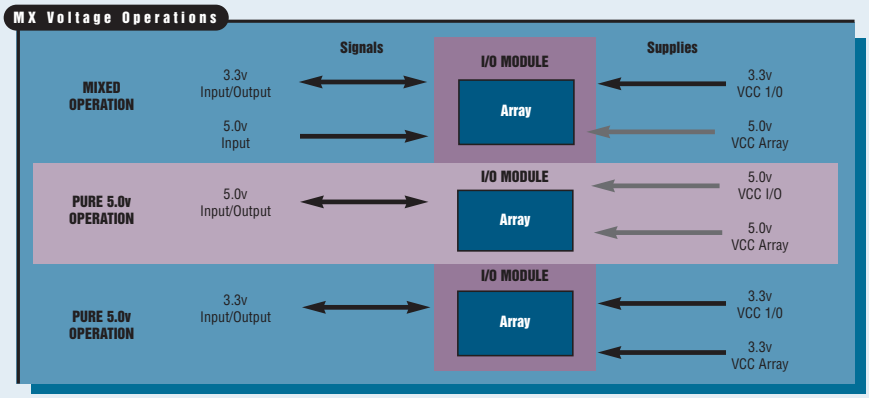
MX-FPGAs

Price/Performance Leader at 5.0V

With capacities ranging from 2,000 to 36,000 gates, 250MHz system performance, and clock-to-out delays as low as 5.6ns, Actel's MX family of FPGAs offers high performance 5.0V solutions.

A Mixed Voltage Solution

Actel's 42MX family of FPGAs includes MultiPlex I/O, an architectural feature that supports mixed-voltage systems and delivers high performance operation at 5.0V.



42MX FPGAs can operate in 5.0V only systems, 3.3V only systems, and mixed 5.0V/3.3V systems, which allows for 5.0V input tolerance in a 3.3V system while providing maximum internal performance. This feature provides flexibility when working with mixed-voltage systems by ensuring compatibility between devices of different voltages.

PCI Compliant

MultiPlex I/O also features chipwide selectable PCI output drives, enabling 100% PCI compliance for both 5.0V and 3.3V I/O systems. In systems that do not require PCI, the PCI output drivers can be disabled to minimize switching currents.

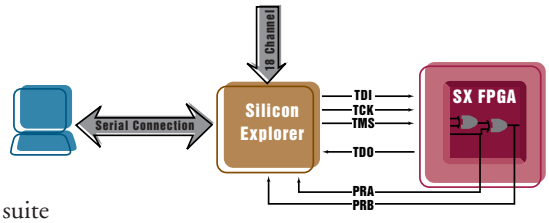
Embedded Dual-Port SRAM

42MX devices contain embedded dual-port SRAM modules. With a 5ns access time, this device family allows designers to build on-board FIFOs and buffers with up to 100MHz performance. These SRAM modules have been optimized for synchronous and asynchronous applications. The modules are arranged in 256-bit blocks that can be configured 32x8 or 64x4. They can also be cascaded together to form memory spaces of user-definable width and depth. The 42MX dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring fast FIFO or LIFO queues.

MX Applications

- *POS Terminal application used 1 MX09 to replace over 20 ICs. Over 16,000 MX devices have shipped in the product.*
- *An HDSL application migrated to a lower cost and high performance MX device, enabling the customer to cancel plans to convert to an ASIC.*
- *A flight controller system used Actel's software and an MX16 to meet density and performance requirements and production commitments in ten weeks.*

Design Tools



Design Services — The One Stop Design Solution

With a ten-year history of providing hardware and software services, Actel's *Protocol* Design Services group offers its customers design support at all stages of project development. With extensive knowledge of FPGA design and prototyping, services are delivered on time, within budget, and to the customers' specifications.

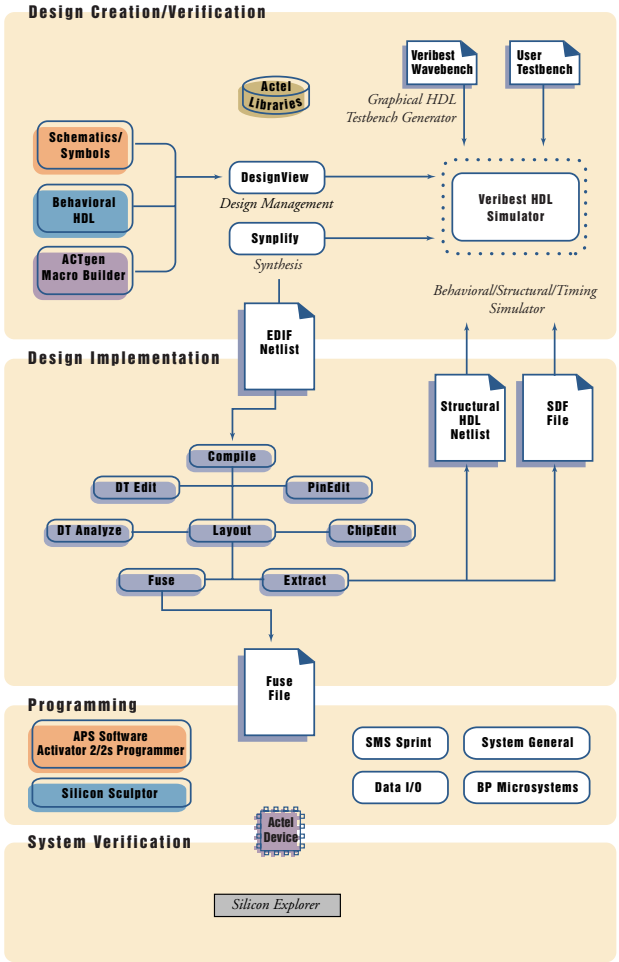
Development Software

The DeskTOP series brings together the best in silicon, synthesis, and simulation to create a complete and integrated design environment for designing Actel FPGAs. The basic **DeskTOP** is an integrated development environment, including simulation, synthesis, and place and route tools, for designs less than 50K gates.

DeskTOP Pro increases the design simulation limit to 400K with unlimited synthesis, allowing designers to move up as their skills and density requirements increase.

DeskTOP Open, which includes simulation up to 400K, and place and route tools, is ideal for ASIC designers who are starting to use FPGAs in their designs, but have already invested in synthesis tools.

Designer Advantage is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTmap VHDL Synthesis tool, ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and the Silicon Sculptor and APS device programming software.



Real-time Device Verification

Actel's antifuse FPGAs contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use verification and logic analysis tool for the PC. Silicon Explorer allows designers to complete the design verification process at their desks.

Programming

Actel offers many programming options, including Activator and Silicon Sculptor single site and multi-site device programmers for PC and UNIX. And when the design is ready to go to production, Actel has a programming solution for that too. Actel offers volume programming services, through Distribution partners.

SX FPGA Family Selector Guide

Part Number	A54SX08	A54SX16	A54SX16P	A54SX32	A54SA72*
Capacity (Gates)	8,000	16,000	16,000	32,000	72,000
JTAG	YES	YES	YES	YES	YES
PCI Compliant	-	-	33MHz, 66MHz	-	33MHz, 66MHz
Maximum I/O	130	177	177	249	360
Dedicated Flip-Flops	256	528	528	1080	2012
Logic Modules	768	1452	1452	2880	6036

*Available Q3 1999

MX FPGA Family Selector Guide

Part Number	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
Capacity (Gates)	2,000	4,000	9,000	16,000	24,000	36,000
Mixed Voltage	-	-	YES	YES	YES	YES
PCI Compliant	-	-	-	-	YES	YES
Maximum I/O	57	69	104	140	176	202
Dedicated Flip-Flops	147	273	348	624	954	1230
Logic Modules	295	547	684	1232	1890	2438
Dual-Port SRAM Bits	-	-	-	-	-	2560

MX/SX PCI Cores

Core	Speed	Width
Target	33MHz (0 wait) 66MHz (0 wait)	32-bit 64-bit
Target +DMA	33MHz (0 wait)	32-bit 64-bit
Master	33MHz (0 wait)	32-bit 64-bit

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