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DSP Builder with Stratix

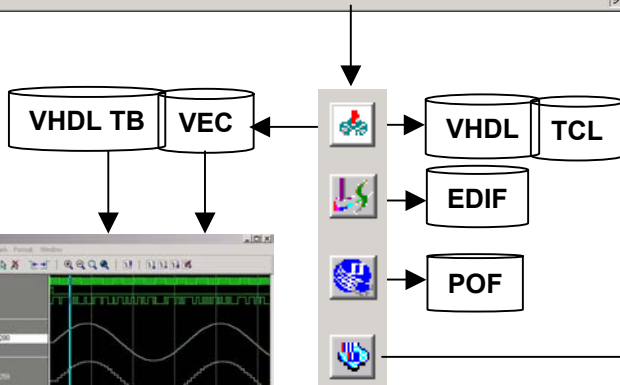
Agenda

- Overview
- DSP Builder Version 2.1.0 Key Features
 - Stratix™ DSP Development Kit
 - Filtering & QPSK Modem Reference Designs
 - Stratix™ GX & ACEX® 2K Devices
 - Multi-Clock Support
 - MathWorks Release 13
- Roadmap

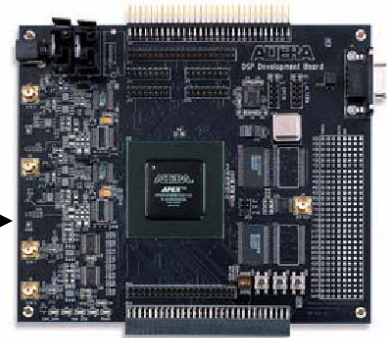
DSP Builder Overview

64 QAM I/Q Modulator
 Oscillator SFDR : 110 db
 Intermediate Freq : 25 MHz
 Root Raised Cosine Filter : roll-off factor = 0.22
 Output QAM Signal Sample rate :200 MSPS

Simulink Library Browser
 Connects to the active-low input switch on the APEX version).



Altera Quartus II
 Compilation progress and timing analysis graphs.



DSP Builder 2.1.0

■ Key Features

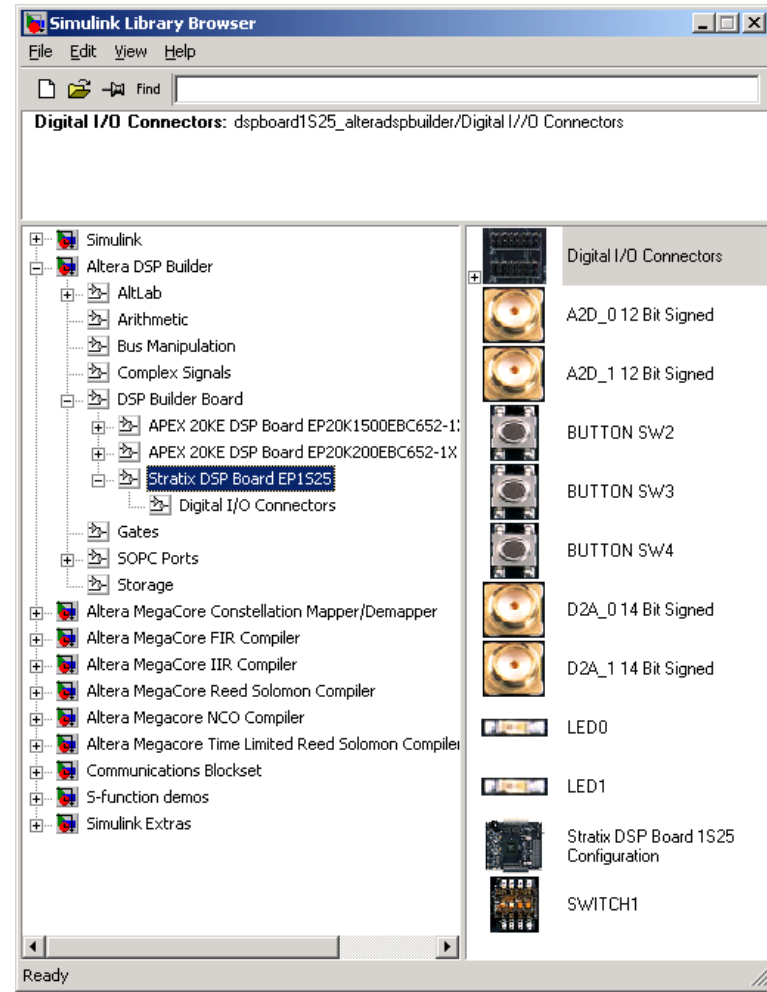
- Stratix DSP Development Kit
 - Filtering & QPSK Modem Reference Designs
- Stratix GX & ACEX 2K
- Multi Clock Support
- MathWorks Release 13

■ Current Schedule Release

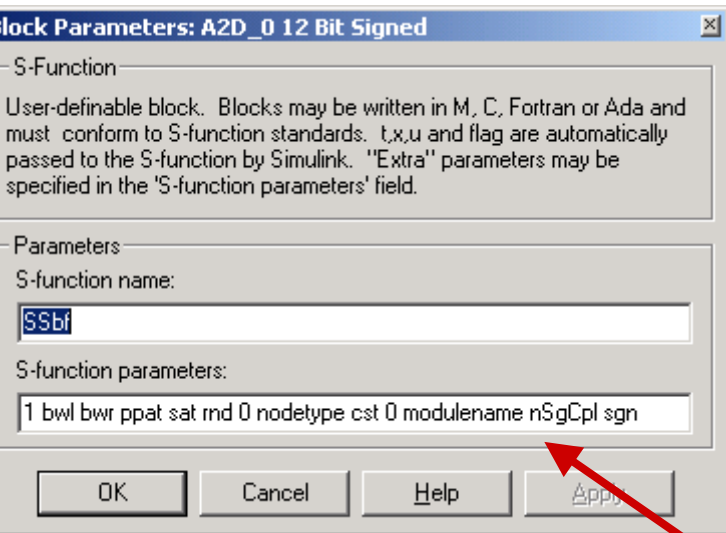
- Production: WW39
- Beta: Now
 - Contact Tapan Mehta (tmehta@altera.com)

Stratix DSP Board

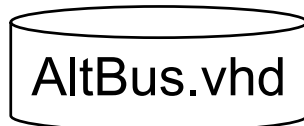
- Board Configuration Block
 - Global Reset
 - Clock
- Connectors :
 - AD, DA, Switches, LED
 - 7 Segment Display
- On Board Memory Interface



Generic Support for DSP Boards



BUTTON SW2

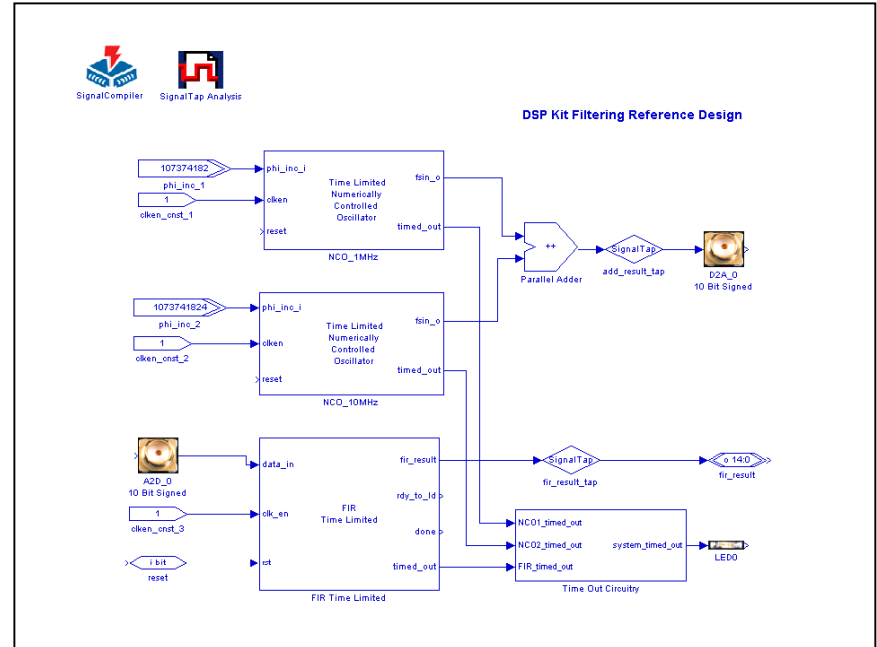


```
*****
* Component (12) : SWITCH4
param(12).sgn                = 'Single Bit';
param(12).nodetype          = 'Input Port';
param(12).bwl               = '1';
param(12).bwr               = '0';
param(12).sat               = 'off';
param(12).rnd               = 'off';
param(12).cst               = '0';
param(12).LocPin            = 'PIN_M26';
param(12).image             = 'switch.bmp';
param(12).componentid      = 'SWITCH4';
param(12).vis               = {'off','off','off','off','off','off'};
*****
* Return Parameter
set_param(gcb,'MaskSelfModifiable','on');
vis                = param(IoComponent).vis;
vis(11)            = 'off';
vis(12)            = 'off';
vis(13)            = 'off';
boardim            = param(IoComponent).image;
genstim            = 'off';
set_param(gcb,'sgn', param(IoComponent).sgn);
set_param(gcb,'nodetype', param(IoComponent).nodetype);
set_param(gcb,'bwl', param(IoComponent).bwl);
set_param(gcb,'bwr', param(IoComponent).bwr);
set_param(gcb,'sat', param(IoComponent).sat);
set_param(gcb,'rnd', param(IoComponent).rnd);
set_param(gcb,'cst', param(IoComponent).cst);
set_param(gcb,'LocPin', param(IoComponent).LocPin);
set_param(gcb,'componentid', param(IoComponent).componentid);
set_param(gcb,'MaskVisibilities',vis);
set_param(gcb,'nSgCpl', num2str(IsSignalCompiler(1)));
set_param(gcb,'ppat','');
if (IsSignalCompiler(1)>0)
    sgncmp = [bdroot '/' 'SignalCompiler'];
    set_param(gcb,'ppat',get_param(sgncmp,'workdir'));
    genstim = get_param(sgncmp,'vstim');
end
```



Reference Designs

- Filter Reference Design
 - NCO, FIR, Signal Tap
 - Stratix DSP Blocks, Stratix DSP Board
- QPSK Modem Reference Design
 - Modulator Demodulator
 - Viterbi, Reed Solomon, Filter, NCO, IIR

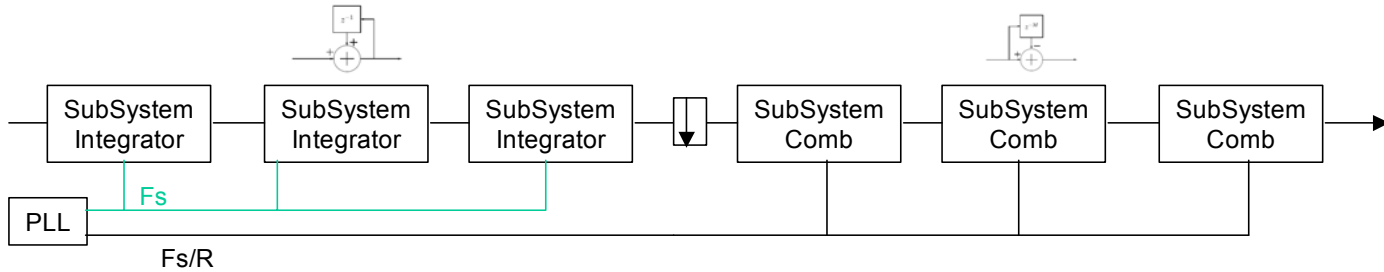


PLL Block

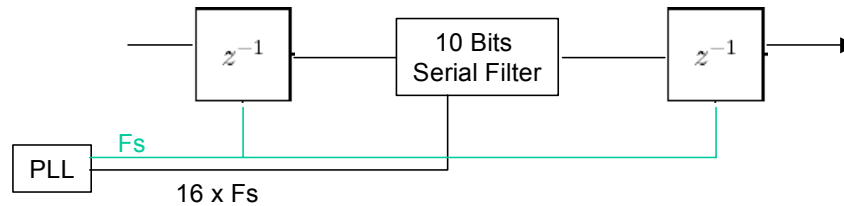
- DSP Builder 1.0.0/2.0.0 Uses One Clock Domain
- DSP Builder 2.1.0 Add Multi-Clock Support via Device PLL to Improve Implementation of Multi-Rate Designs
 - CIC Filters
 - Multi-Bit Filters
 - TDM Streaming Data Path Design
- Up to 6 Clocks with PLL
- Devices that Contain PLLs
 - Stratix, GX, APEX™ & ACEX 2K Devices
- If Multi-Clock Block Not Used
 - Design Reverts Back to Normalized Nyquist (Version 2.0)

Multi-Rate Designs Example

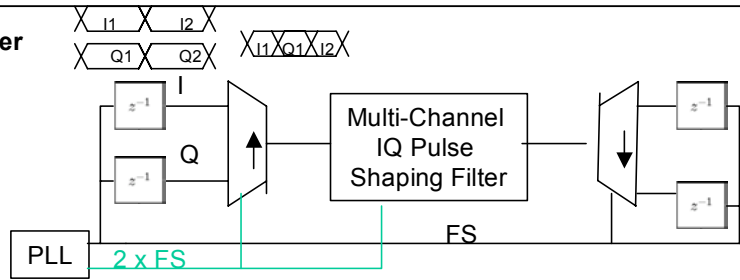
3 Stage Decimating CIC Filter with Rate Changing R



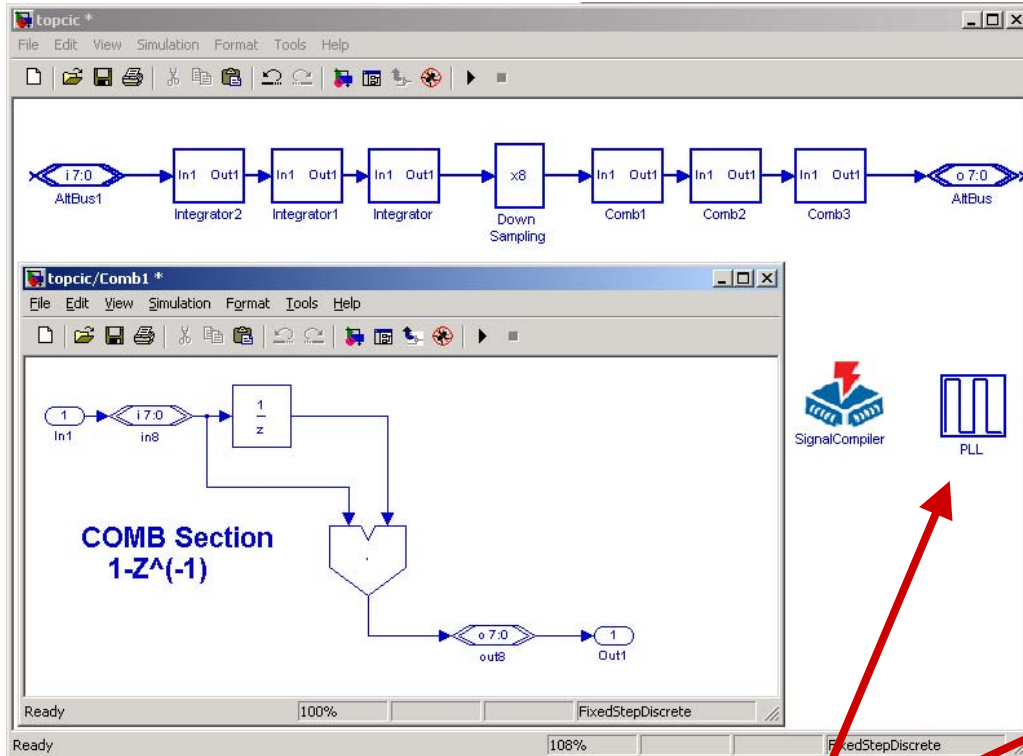
Streaming Serial Filter



IQ MultiChannel Filter



Step 1 : Setting PLL Parameters



DSP Builder - Multi Clock Setting

PLL Clock Setting

clk0	10 ns	(100 Mhz)	
clk1	1 / 8	(12.5 Mhz)	PLL (Clk0)
clk2	1 / 1	(100 Mhz)	Unused
clk3	1 / 1	(100 Mhz)	Unused
clk4	1 / 1	(100 Mhz)	Unused
clk5	1 / 1	(100 Mhz)	Unused

Buttons: OK, Help, Cancel

New DSP Builder
PLL Block
Using altclklock.vhd

Step 2 : Setting Blocks Sample Time

The image displays three overlapping windows from the Altera Quartus II software:

- topcic ***: A block diagram showing a signal path from an **AltBus1** through three **Integrator** blocks, a **Down Sampling** block ($\times 8$), and three **Comb** blocks, ending at **AltBus**.
- topcic/Comb1 ***: A zoomed-in view of a **COMB Section** block, showing an input **In1** and an output **in8**.
- Block Parameters: Delay**: A dialog box for configuring a delay block. The **Delay** parameter is set to 1. The **Clock Source** dropdown menu is open, showing options **clk0**, **clk1**, **clk2**, and **clk3**. A red arrow points from the **COMB Section** block in the previous window to this dialog.
- Simulation Parameters: untitled**: A dialog box for simulation settings. The **Fixed step size** is set to **1e-6**, which is circled in red. A red arrow points from this value to the text box below.

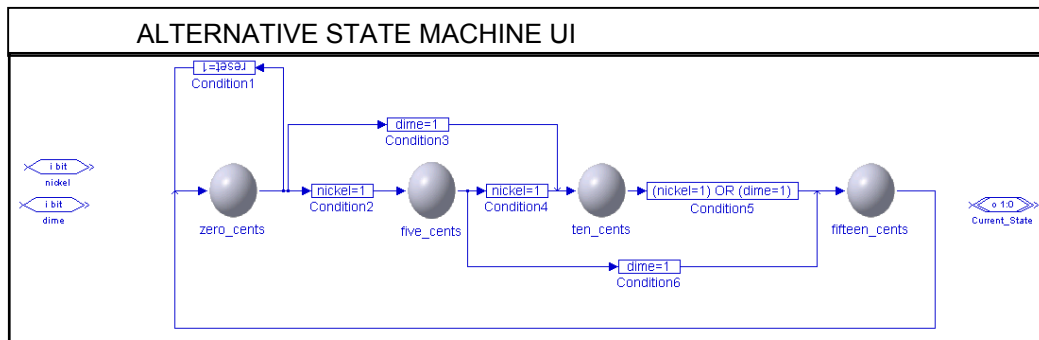
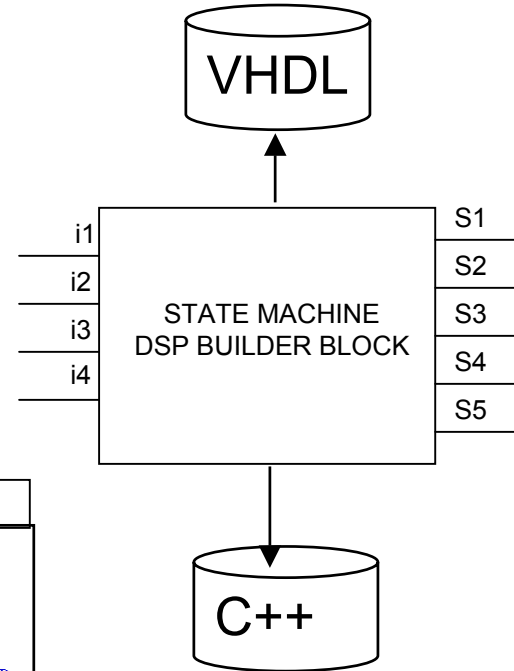
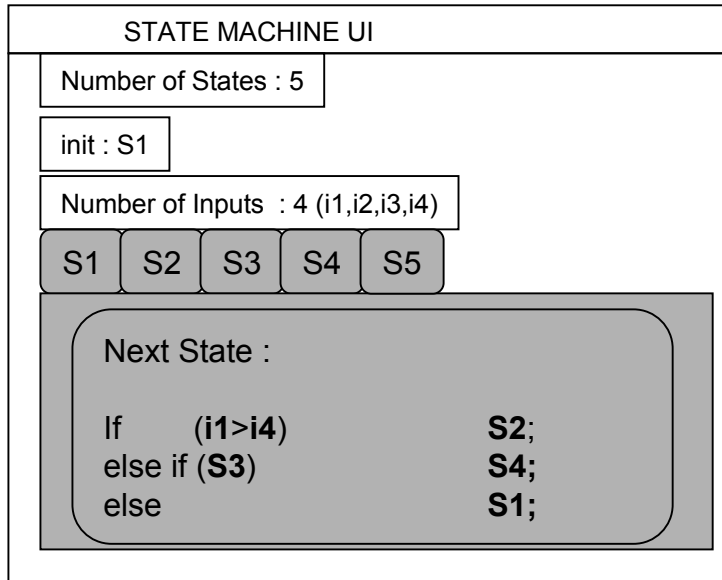
**Registers & Subsystems have a Clock Source Option
Default is clk0**

**Simulation Will Actually be Reference to a Time Period
Currently Designs Are Normalized to Sample Rate of 1 (Highest Clock)**

Controller Block

- Enhance DSP Builder Control Capabilities over existing IF-THEN-ELSE & CASE-STATEMENT Blocks
- Provide Menu-Driven Block to System-Level Engineer to Design Simple Controller or State Machine
- Controller Block Output States Bits Based on Inputs Conditions
- Moore Type State Machine

Controller Block



Controller- State Machine -



```
static void mdlStart(SimStruct *S, int_T tid)
{
    ssGetPWork(S)[0] = (void *) new Controller(nState,
*Condition);
}

static void mdlOutputs(SimStruct *S, int_T tid)
{
    Controller *pController = (Controller *) ssGetPWork(S)[0];
    for (i=0;i<nState;i++){
        real_T *y = ssGetOutputPortRealSignal(S,i);
        y[i] = pController->GeState(i);}
}

#define MDL_UPDATE
static void mdlUpdate(SimStruct *S, int_T tid)
{
    Controller *pController = (Controller *) ssGetPWork(S)[0];
    for (i=0;i<nInput;i++){
        InputRealPtrsType inpt =ssGetInputPortRealSignalPtrs(S,0);
    }
    pController->NextClock(ce,cl,inpt);
}

static void mdlTerminate(SimStruct *S)
{
    Controller *pController = (Controller *) ssGetPWork(S)[0];
    delete pController ;
}
```

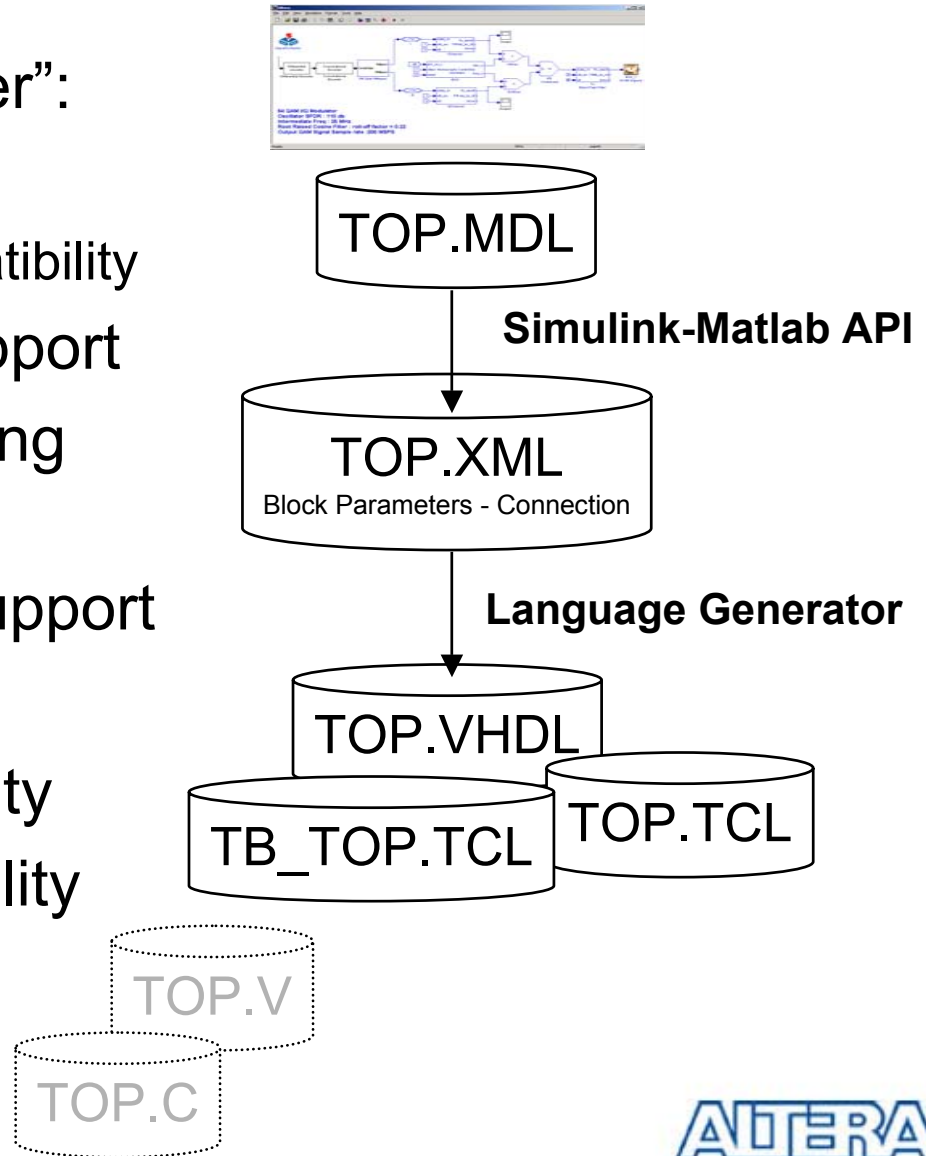
```
combin: process (CURRENT_STATE, X)
begin
    case CURRENT_STATE is
        when s0 =>
            if X = '0' then
                NEXT_STATE <= s0;
            else
                NEXT_STATE <= s2;
            end if;
        when s1 =>
            if X = '0' then
                NEXT_STATE <= s0;
            else
                NEXT_STATE <= s2;
            end if;
        when s2 =>
            if X = '0' then
                NEXT_STATE <= s2;
            else
                NEXT_STATE <= s3;
            end if;
        when s3 =>
            if X = '0' then
                NEXT_STATE <= s3;
            else
                NEXT_STATE <= s1;
            end if;
    end case;
end process;
-- Process to hold synchronous elements (flip-flops)
sync: process
begin
    wait until CLOCK'event & CLOCK = '1';
    CURRENT_STATE <= NEXT_STATE;
end process;
end BEHAVIOR;
```

MathWorks Release 13

- Add MathWorks Release 13 Eval CD in Stratix DSP Kit
- August 2002
 - Matlab 6.5
 - Simulink 5.0
- Modeling for Wireless, Mechanical, & Power System
- Intrinsic Fixed-Point
- Next Generation of Automatic Production Code
 - Embedded Target for Motorola® MPC555
 - Embedded Target for C6000™ DSP Platform
- Targeting for Microcontrollers, DSPs, & FPGAs

DSP Builder – Simulink 5.0

- Enhanced “SignalCompiler”:
 - Use Matlab API
 - Ensure Forward Compatibility
 - Multiple Language Support
 - Enhanced Error Tracking Messages
 - Improved Hierarchy Support
- Regression Test
 - C++ Model Compatibility
 - Simulink UI Compatibility



Quartus II 2.1

- New Device Families
 - Stratix GX
 - ACEX 2K
 - Excalibur™
- Support Native VHDL Synthesis
 - Signal Compiler UI / Documentation
 - SignalTap
- Adding Support to Program Device with SOF File Outside Quartus® II Software in Addition Using The Jam Player (Quartus II 2.1 SP1) for OpenCore®+.

Bug Fixes

- DSP Builder SPR Bug Fixes/Enhancement
 - Unlimited Number of Sub-Hierarchies
 - Enhance Parallel Adder Functionality
 - Look Up Table (LUT) for Stratix in ROM Mode
 - Installation
 - AltBus in Constant Mode
 - APEX DSP Board Pinout

Roadmap

- Generating Simulink Model from Quartus II
- Inject Stimuli to the Board
- Verilog Support
- Unix Support
- Mathematical Operator Extension
 - Floating-Point Operator
 - Galois Field Operator
 - Vectorized Math (Matrix/Array Operation)
- SOPC Links Enhancements
 - Custom Instructions

Roadmap (Con't)

- Support for Simulink Plug-In
 - Real Time WorkShop (C Generation for Processor)
 - Fixed-Point BlockSet
 - State Flow
- VisSim (MathCad), Elanix, SPW
- Calling Quartus Simulation Engine from Simulink Simulation for Timing Simulation



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Stratix DSP Development Kit

Overview

■ Hardware

- Stratix DSP Development Board (EP1S25)
 - Ordering Code: DSP-BOARD/S25
 - List Price: \$1,995

■ Software

- Quartus II
- DSP Builder
- 30-Day MATLAB/Simulink Evaluation Copy

■ Several System Reference Designs

Improved Over APEX DSP Kit

- New Features  **New**
 - Support for Nios[®] + DSP Hardware Acceleration
 - High Speed Link from DSP Board into DSP Builder for Hardware Evaluation
 - Standard Expansion Connectors for TI TMS320 Development Kit & Analog Devices ADC Evaluation Boards
 - Improved Features
 - Stratix EP1S25F780 Device
 - Faster, Higher Resolution Data Converters
 - 2 Channel 12-Bit, 125 MSPS A/D
 - 2 Channel 14-Bit, 165 MSPS D/A
 - More System Reference Designs

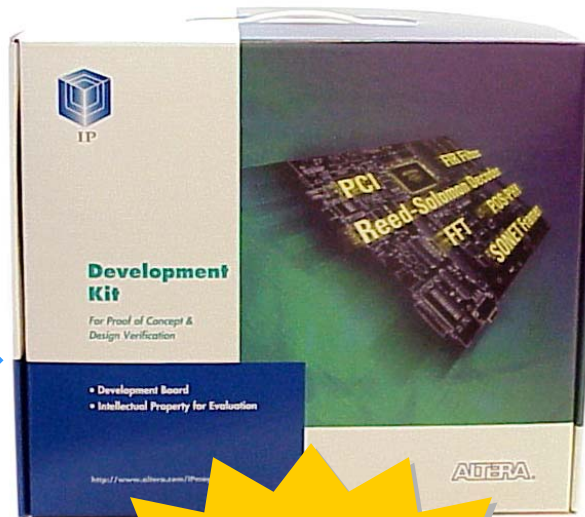
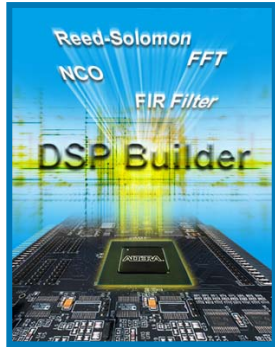
Stratix DSP Board – Key Features

- Stratix EP1S25F780 Device
- Analog I/O
 - 2 Channel 12-Bit, 125 MSPS A/D
 - 2 Channel 14-Bit, 165 MSPS D/A
- Digital I/O
 - Four 40-pin Connectors for Analog Devices A/D Converter Evaluation Boards
 - Connector for TI TMS320 Cross-Platform Daughter Card
 - 3.3V Expansion/Prototype Headers
 - RS 232 Serial Port
- 2 Mbytes of 7.5ns Synchronous SRAM

Stratix DSP Development Kit

Available
ww 46

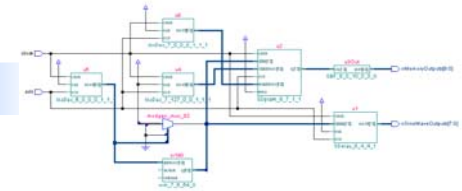
Contains Everything User Needs
to Develop High-Performance DSP
Designs on PLDs



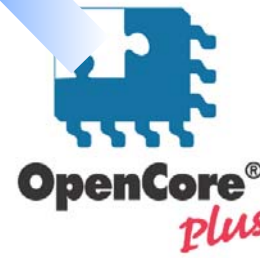
Starter Version
for \$1,995 Only



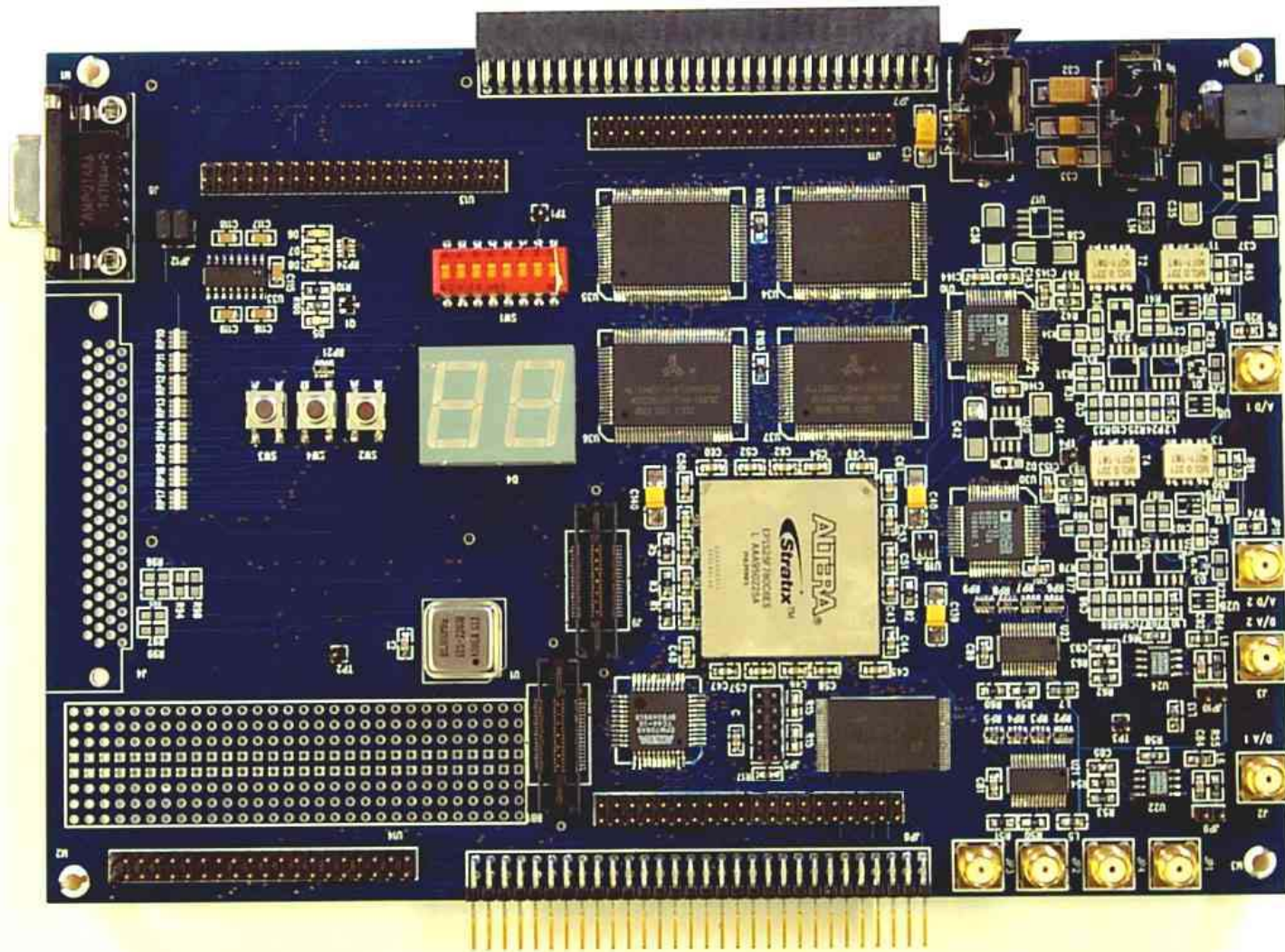
30 Day Evaluation
Copy



System Reference
Designs



Stratix DSP Development Board



Complete Kit Deliverables

■ Hardware

- Stratix DSP Development Board
- ByteblasterMV Cable
- SMA Cable
- RS232 Cable
- Power Supply Adapter

■ Software

- Quartus II
- DSP Builder
- 30-Day Simulink Evaluation Copy

■ Reference Designs

- Filtering
- QPSK Modem
- Digital Down Converter
- Direct Sequence Spread Spectrum (DSSS)

■ Documentation

- Quick Start Guide
- DSP CD-ROM
 - DSP Board Data Sheets
 - OpenCore Plus Hardware Evaluation Application Note
 - OpenCore Plus Hardware Evaluation Executables

DSP Kit Reference Designs

- Design #1: Simple Demo
 - Programmed into Flash
 - Enables User to Test LEDs, Seven Segment LCD, DIP Switches & Push-Button Switches
 - Provide .pof file with Demo

DSP Kit Reference Designs (Cont.)

- Design #2: Filtering in DSP Builder
 - Provide *Out-of-Box* Experience Showing Off Key Features of Kit
 - Any FAE Should Be Able to Demo Kit
 - Use Stratix DSP Blocks, DSP IP, DSP Builder, & Signal Tap Readback
 - Generate 2 Sine Waves with NCO, Send Out D/A, Loopback through A/D, & Filter Signal Using FIR
 - Read Output Back Thru SignalTap Readback & Plot Filtered Output Next to Original Signal
 - Perform FFT on Signals in Matlab to View Input/Output in Frequency Domain
 - OpenCore+
 - Lab Included (Walk-Thru)

DSP Kit Reference Designs (Cont.)

- Design #3: Single Channel QPSK Modem in DSP Builder
 - Provide More Advanced Design as Training Vehicle for DSP Builder & DSP IP & Highlights High-Performance Capabilities of Stratix Where Possible
 - Key Blocks
 - Downconverter/Upconverter
 - FEC – Concatenated Viterbi/Reed Solomon with Interleaver
 - Modulation – QPSK
 - OpenCore+
 - Use Signal Tap Readback
 - Plot BER In Matlab
 - Lab for Each Subsystem & Final Integration
 - Application Note

DSP Kit Reference Designs (Cont.)

- Design #4: Digital Down Converter
 - Production-Level Design Highlighting Stratix & IP Capabilities in as Small A Design as Possible
 - Digital Down Converter with 100+ SFDR Squeezing as Many Channels into 1S25 Device as Possible
 - Show Price/Performance Advantages Versus Graychip 4016
 - Would Like to Adhere as Closely as Possible to UMTS Requirement
 - Output Seen on Scope
 - Application Note (No Lab)

DSP Kit Reference Designs (Cont.)

- Design #5: Direct Sequence Spread Spectrum (DSSS)
 - As Close as Possible to Single-Channel UMTS Design
 - Digital Downconverter/Upconverter Using FIR & NCO
 - Spreading/Despreading
 - QPSK Mapping with Constellation Mapper/Demapper
 - Correlator for Synchronization
 - Loopback from D/A to A/D
 - AGC
 - Signal Tap Read Back
 - Application Note

Pricing & Availability

■ Pricing

- Ordering Code: DSP-BOARD/S25
- List Price: \$1,995

■ Availability

- Production: WW46

Conclusion

- DSP Development Kit – Complete Development System Enables Engineers to Use Programmable Logic for DSP Designs
- Shortens Design Development Time, Which Leads to Faster Time to Market
- Offers Complete Integrated Platform for Easy Prototyping & Debugging
- Enables Designers to Test IP Cores in Silicon Prior to Licensing